Remarks

Applicant respectfully requests reconsideration of this application. Claims 1-5 and 34-44 are pending. No claims have been allowed.

Claim 1 has been amended, not substantively, but rather for stylistic preferences to improve the form of the claim. The claim amendments merely make explicit what was already implicit in applicant's specification and drawings. Therefore, it is expected that the claims will be entitled to a full range of equivalents.

Double Patenting

Claims 1-5, 34-44 stand provisionally rejected as claiming the same invention as that of claims 6-59 of copending Application No. 10/278,551 filed 10/22/02. Since the issue fee in this copending case was paid on 11/25/03, Applicant is submitting herewith a terminal disclaimer in compliance with 37 CFR § 1.321(c) to overcome the provisional rejection.

Claim Rejections - 35 U.S.C. § 102(b)

Claims 1-5, 34-44 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Baliga (US 5,998,833; "Baliga").

Baliga discloses an integrated power semiconductor device with a drift layer 112 and a method of fabricating the same. As illustrated in Figure 3, Baliga teaches a device having a gate electrode/source electrode insulating region 125, a gate electrode 127 and a trench-based source electrode 128a formed below the gate electrode in the trench. Baliga discloses a method of fabrication of his device structure in Figures 4A-4K, which includes the steps of forming trenches in an epitaxial layer and forming insulating regions on the vertical sidewalls of the trenches. However, Baliga fails to teach or disclose "filling a remaining portion of the trenches with a conductive material to form first and second field plate members" as

recited in claim 1, for example. Instead, Baliga teaches forming a trench-based source electrode 26 by partially filling the bottom of his trench, followed by an etching step to remove the insulating regions 24 from the sidewalls. Next, a second insulating region is formed followed by a conformal polysilicon deposition to form gate member 30 in a top portion of the trench. (Col. 10, lines 1-29).

The Office Action states that Baliga discloses a method of fabrication an extended drain region of a high-voltage transistor in Figs. 4A-4K that includes "filling a remaining portion of the trenches with a conductive material 26, 28, 126 to form first and second field plate members 136, 138 that are insulated from the substrate 10 and the epitaxial layer 12." Applicant respectfully submits that the Examiner misreads the reference since Baliga's regions 28 and 138 are disclosed as insulating regions (e.g., col. 10, lines 5-12; 45-55), not field plate members formed of a conductive material.

Moreover, with respect to the fabrication sequence shown in Figs. 4A-4K, the processing steps disclosed relate to the formation of Baliga's source electrode 26 and gate member 30, which are clearly not the same as Applicant's claimed first and second field plate members. In other words, there is no disclosure or teaching in Baliga of a process for forming first and second field plate members of a conductive material insulated from the first and second sidewall portions of the mesa, as per claim 34, for example. Baliga does disclose a field plate 136 provided on a field plate insulating region 134 in his device of Figure 5, but he provides no teaching or disclosure about the method of fabrication. Moreover, it is evident from Figure 5 that Baliga's field plate 136 is disposed only on one side of a mesa transition region that terminates his device cell at the edge. In other words, Baliga fails to teach or disclose forming first and second field plate members in trenches disposed on opposite sides of a mesa that forms an extended drain region of a device.

Consequently, it is respectfully submitted that Baliga does not anticipate the invention of claims 1-5, 34-44.

Accordingly, Applicant respectfully submits that the claims 1-5, 34-44 are in condition for allowance.

Please charge any shortages and credit any overcharges to our Deposit Account No. 50-2060.

Respectfully submitted,

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